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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,494	12/09/2003	Arvind Halliyal	AF01194	4623

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EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,494	HALLIYAL ET AL.	
	Examin r	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-10,12-15 and 17-20* is/are rejected.

7)☒ Claim(s) *2,7,11 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 8, 9, 10, 17 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al., U.S. Patent 6,767,796 B2.

Tanaka discloses a semiconductor process as claimed. See **FIGS. 1A-24**, where Tanaka teaches the claimed limitations.

FIG.11A

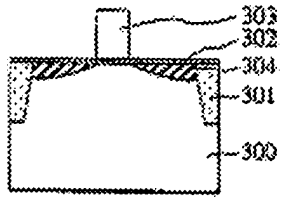
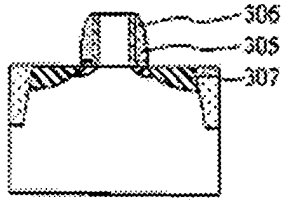


FIG.11B



4. Pertaining to claim 1, Tanaka teaches a process for fabricating a semiconductor device comprising:

providing a semiconductor substrate **300** having formed thereon a semiconductor device (not numbered, however, a gate insulator **302**, gate electrode **303** and source drain **307** are disclosed as what is known as a MOSFET);

depositing over the semiconductor device a spacer layer **305/306**, the spacer layer having a first hydrogen content (see **FIG. 17**); and

applying a treatment to reduce the first hydrogen content to a second hydrogen content.

5. Pertaining to claim 8, Tanaka teaches the process of claim 1, wherein the treatment is applied to the spacer layer, prior to etching to form a spacer for the semiconductor device (the Examiner takes the position that the first sidewall layer is the on formed after the ldd is formed and activated).

6. Pertaining to claim 9, Tanaka teaches the process of claim 1, wherein the process further comprises a step of etching to form a spacer for the semiconductor device, and the treatment is applied to the spacer subsequent to the etching step.

Pertaining to claim 10, Tanaka teaches a process for fabricating a charge trapping dielectric flash memory device comprising:

providing a semiconductor substrate having formed thereon a gate stack comprising a charge trapping dielectric charge storage layer and a control gate electrode overlying the charge trapping dielectric charge storage layer;

depositing over the gate stack a spacer layer, the spacer layer having a first hydrogen content; and applying a treatment to reduce the first hydrogen content of at least a portion of the spacer layer to a second hydrogen content (see the art rejection as applied to claim 1 above and **FIGS.23A-23B**).

7. Pertaining to claim 17, Tanaka teaches the process of claim 10, wherein the treatment is applied to the spacer layer, prior to an etching step for forming a gate stack spacer.

8. Pertaining to claim 18, Tanaka teaches the process of claim 1, wherein the treatment is applied to the gate stack spacer subsequent to an etching step for forming a gate stack spacer.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3, 4, 5, 6, 12, 13, 14, 15, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al., U.S. Patent 6,767,796 B2.

11. Tanaka discloses a semiconductor process substantially as claimed. However, Tanaka fails to disclose the atomic percentage of hydrogen left in the sidewall spacers as claimed. Given the teachings of what is disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. "*In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Objections

12. Claims 2, 7, 11 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on 9:00 AM-5:00 PM.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC